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| 10/593,386 | 12/04/2006 | John Fleming Walker | 7251/96026 | 8885 |

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| EXAMINER | |
|---|---|
| LE, DUNG ANH | |

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| 2818 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/593,386 | WALKER, JOHN FLEMING | |
| | Examiner | Art Unit | |
| | DUNG A. LE | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22 and 25-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 25-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/13/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

## Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 11/13/2006 has been considered and made of record. The references cited on the PTOL 1449 form have been considered.

## Specification

The specification is objected to for the following reason:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP § 606.01).

Note that, the claims are directed to a method of making a semiconductor device instead of to a semiconductor device.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## Drawings

The drawings are objected to for the following reasons.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show "a first portion of an additional layer", "a second portion of an additional layer", "a first integrated circuit" and "a second integrated circuit" as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required.

## Claim Rejections

### Claim Rejections - 35 USC § 112

Claims 6, 13, 17 and 22 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant(s) is reminded that the presence of process limitations on product claims, which product does not otherwise patentability distinguish over prior, cannot impart patentability to the product. In re Stepens 145 USPQ 656 (CCPA 1965). The process steps in claim 6, which include a integrated circuit has not been given patentably weight. The process steps in claim 13, which include a plurality of integrated circuits and has not been given patentably weight. The process steps in claim 17, which include a integrated circuit has not been given patentably weight. The process steps in claim 13, which include a plurality of integrated circuits and has not been given patentably weight.

**Set of claims 1-6.**

**Claims 1, 3-5 are rejected under 35 USC 102 (b) as being anticipated by Farrar (6,495,919 B2).**

**Regarding claim 1,** Farra teaches a method for adding an additional layer to an integrated circuit, the method comprising:

providing an integrated circuit having an interconnect layer 24;

depositing, over substantially all of an exposed surface of the integrated circuit, an additional layer 14 of material whose conductivity can be altered; and

selectively altering the conductivity of a first portion of the additional layer by selective annealing (col 8, lines 47-63) and (Especially, at least see figures 4-5 and refer to related texts), to produce a sub-circuit in the additional layer 14, the sub-circuit being in operative electrical communication with the integrated circuit.

**Regarding claim 3**, wherein the sub-circuit is not visually distinguishable from a second portion of the additional layer 14, the second portion being disjoint from the first portion 30 (Especially, at least see figures 5-6 and refer to related texts).

**Regarding claim 4,** wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion (Especially, at least see figures 5-6 and refer to related texts).

**Regarding claim 5**, the selectively altering comprises altering substantially without removing any part of the additional layer 14.

**Regarding claim 6**, see 112 rejection as mentioned above.

**Claim 2 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Farra in view of Pankove (4,339,285).**

Farra teaches the claimed invention as applied to claim 1 except for the selective annealing comprises selective laser annealing as cited in current claim.

Pankove shows the selective annealing comprises selective laser annealing (col 2, lines 5-10, lines 35-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the selective annealing comprises selective laser annealing in Farra 's method in order to form a doped portion which is substantially conducting (col 2, lines 8-10).

**Set of claims 7-15**

**Claims 7-8, 10-13 are rejected under 35 USC 102 (b) as being anticipated by Farrar (6,495,919 B2).**

Farra teaches a method for adding an additional layer to a plurality of integrated circuits, the method comprising:

providing a plurality of integrated circuits, each having an interconnect layer 24;

performing the following for each one of the plurality of integrated circuits:

depositing, over substantially all of an exposed surface of the one integrated circuit, an additional layer 14 of material whose conductivity can be altered; and

selectively altering the conductivity of a first portion 30/36 of the additional layer by selective annealing, to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit (Especially, at least see figures 3-5 and refer to related text),

wherein the first portion 30 of each integrated circuit has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit (Especially, at least see figure 5-8 and refer to related texts).

**Regarding claim 8**, wherein the shape of the first portion 30 of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on the production wafer (Especially, at least see figure 8 and refer to related text).

**Regarding claim 10,** the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion 14 (Especially, at least see figures 4-5 and refer to related text).

**Regarding claim 11,** the second portion comprises substantially all parts of the additional layer not comprised in the first portion (Especially, at least see figure 8 and refer to related text).

**Regarding claim 12**, the selectively altering comprises altering substantially without removing any part of the additional layer.

**Regarding claim 13,** see 112 rejection above.

**Claim 9 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Farra in view of Pankove (4,339,285).**

Farra teaches the claimed invention as applied to claim 7 except for the selective annealing comprises selective laser annealing as cited in current claim 9.

Pankove shows the selective annealing comprises selective laser annealing (col 2, lines 5-10, lines 35-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the selective annealing comprises selective laser annealing in Farra 's method in order to form a doped portion which is substantially conducting (col 2, lines 8-10).

**Set of claim 14- 17.**

**Claims 14-16 are rejected under 35 USC 102 (b) as being anticipated by Farrar (6,495,919 B2).**

**Regarding claim 14**, Farrar teaches a method for adding an additional layer (Especially, at least see figures 3-8 and refer to related texts)to an integrated circuit, the method comprising:

providing an integrated circuit having an interconnect layer 24;

depositing, over substantially 14 all of an exposed surface 16 of the integrated circuit, an

additional layer of material whose conductivity can be altered;

selectively doping (col 4, lines 30-35) only a first portion 30 of the additional layer 14 of material; and

selectively altering the conductivity of the first portion of the additional layer by annealing (col 8, lines 45-60), to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit.

**Regarding claim 15**, wherein the sub-circuit is not visually distinguishable from a second portion of the additional layer (Especially, at least see figures 5-6 and refer to related text), the second portion being disjoint from the first portion 30.

**Regarding claim 16**, wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion 14 (Especially, at least see figure 8 and refer to related text).

**Regarding claim 17**, see 112 rejection as mention above.

**Set of claims 18-22.**

**Claims 18-24 are rejected under 35 USC 102 (b) as being anticipated by Farrar (6,495,919 B2).**

**Regarding claim 18**, Farrar teaches a method for adding an additional layer to a plurality of integrated circuits (Especially, at least see figures 3-8 and refer to related texts), the method comprising:

providing a plurality of integrated circuits, each having an interconnect layer 24;

depositing, over substantially all of an exposed surface 16 of each of the plurality of integrated circuits, an additional layer 14 of material whose conductivity can be altered;

for each one of the plurality of integrated circuits, selectively doping (col 4, lines 30-35) and (Especially, at least see figure 4 and refer to related text) a first portion 30 of the additional layer 14 of material of the one integrated circuit; and

selectively altering the conductivity of the first portion of the additional layer of each of the plurality of integrated circuits by annealing (col 8, lines 45-60) , to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit,

wherein the first portion 30 of each integrated circuit has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit (Especially, at least see figure 8 and refer to related text).

**Regarding Claim 19**, wherein the shape of the first portion 30 of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on the production wafer (Especially, at least see figure 8 and refer to related text).

**Regarding claim 20**, the sub-circuit is not visually distinguishable (Especially, at least see figure 6 and refer to related text) from a second portion of the 30 additional layer, the second

portion being disjoint from the first portion.

**Regarding claim 21,** the second portion comprises substantially all parts of the additional layer 14 not comprised in the first portion 30.

**Regarding claim 22**, see 122 rejection as abovementioned.

**Set of claims 25-32**

**Claims 26-26 and 28-32 are rejected under 35 USC 102 (b) as being anticipated by Farrar (6,495,919 B2).**

**Regarding claim 25,** Farra teach a method for producing an integrated circuit, the method comprising:

providing a lower integrated circuit portion 10 including an interconnect layer 24; and

producing an additional layer 14 of material disposed over substantially all of a surface of the lower integrated circuit portion, the additional layer comprising a first portion 30, the first portion comprising a sub-circuit in operative electrical communication with the lower integrated circuit portion, the sub-circuit being not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

**Regarding claim 26**, wherein the producing comprises:

depositing, over substantially all of an exposed surface of the lower integrated circuit

portion, an additional layer 14 of material whose conductivity can be altered; and

selectively altering the conductivity of a first portion of the additional layer 14 by selective annealing, thereby producing the sub-circuit (col 8, lines 47-63).

**Regarding claim 28**, wherein the selectively altering comprises altering substantially without removing any part of the additional layer.

**Regarding claim 29**, wherein the producing comprises:

depositing, over substantially all of an exposed surface of the lower integrated circuit portion 10, an additional layer 14 of material whose conductivity can be altered;

selectively doping only a first portion 30 of the additional layer of material; and

selectively altering the conductivity of the first portion of the additional layer by annealing (col 8, lines 47-63).

**Regarding claim 30**, wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion (Especially, at least see figures 5-6 and refer to related text).

**Regarding claim 31**, wherein the first portion 30 has a shape, and, for at least a first integrated circuit and a second integrated circuit of a plurality of integrated circuits on a production wafer, the shape of the first portion of the first integrated circuit is different from the

shape of the first portion of the second integrated circuit (Especially, at least see figures 7-8 and refer to related texts).

**Regarding claim 32,** wherein the shape of the first portion 30 of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on a production wafer (Especially, at least see figures 7-8 and refer to related texts).

**Claim 27 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Farra in view of Pankove (4,339,285).**

Farra teaches the claimed invention as applied to claim 25 except for the selective annealing comprises selective laser annealing as cited in current claim.

Pankove shows the selective annealing comprises selective laser annealing (col 2, lines 5-10, lines 35-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the selective annealing comprises selective laser annealing in Farra 's method in order to form a doped portion which is substantially conducting (col 2, lines 8-10).

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Lock can be reached on (571) 272-1657. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DUNG A LE/
Primary Examiner, Art Unit 2818